An, wherein n = 0, 1, ... 11, and bank address signals BA0 and BA1, a control signal generation circuit 2003 receiving an output of input buffer 2001 to generate an internal control signal, a row address latch 2004 responsive to the internal control signal for latching a row address output from input buffer 2002, a column address latch 2005 responsive to the internal control signal for latching a column address output from input buffer 2002, a memory array 2006 having a plurality of memory cells arranged in rows and columns, and a plurality of word lines arranged in the direction of the rows and a plurality of bit lines arranged in the direction of the columns, a row decoder 2007 responsive to the internal control signal for selecting a row corresponding to an output of row address latch 2004, and a column decoder 2008 responsive to the internal control signal for selecting a column corresponding to an output of column address latch 2005. Input buffers 2001 and 2002 take a received signal in in synchronization with clock BUFFCLK (or CLKin3) output from DLL 2000. Clock CLKin3 is more suitable for rapid operation than clock BUFFCLK.--

IN THE CLAIMS:

Please amend claim 1 as follows.

1. A delay locked loop comprising:

a delay circuit delaying a first clock to output a second clock;

a detector detecting a phase difference between said first and second clocks; and

a gray code counter using a gray code, responsive to an output of said detector for generating a signal adjusting an amount of delay of said delay circuit.